AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 2, 4, 7, 9 and 11, amend claims 1 and 6 and add newly written claims 12 and 13 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) Apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

at least one further circuit, responsive to said performance control signal, to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit supports data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change, wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels, and, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

2. (cancelled).

3. (original) Apparatus as claimed in claim 1, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

4. (cancelled).

5. (original) Apparatus as claimed in claim 1, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.

6. (currently amended) A method of processing data, said method comprising the steps of:

performing data processing operations with a processor, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

in response to said performance control signal, operating one or more further circuits so as to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said operating step includes supporting data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at

least one intermediate data processing performance level during said change, wherein said one or more further circuits include a voltage controller operable to generate a power signal for said processor at a plurality of different voltage levels, and, in response to an increase in desired data processing performance level, said clock generator increases clock signal frequency to an intermediate clock signal frequency when said voltage controller is generating a power signal with a voltage level sufficient to support said intermediate clock signal frequency.

7. (cancelled).

8. (original) A method as claimed in claim 6, wherein said one or more further circuits include a clock generator operable to generate a clock signal with a selectable clock frequency.

9. (cancelled).

10. (original) A method as claimed in claims 6, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.

11. (cancelled).

12. (new) Apparatus for processing data, said apparatus comprising:

a processor operable to perform data processing operations, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

at least one further circuit, responsive to said performance control signal, to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said at least one further circuit supports data processing of said processor at at least one intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.

13. (new) A method of processing data, said method comprising the steps of:

performing data processing operations with a processor, said processor being operable to generate a performance control signal indicative of a desired data processing performance level of said processor; and

in response to said performance control signal, operating one or more further circuits so as to support said desired data processing performance level of said processor; wherein while responding to a change in performance control signal corresponding to a change from a first desired data processing performance level to a second desired data processing performance level, said operating step includes supporting data processing of said processor at at least one

intermediate data processing performance level and said processor temporarily operates at said at least one intermediate data processing performance level during said change, wherein one or more priority signals serve to trigger said further circuit change to support a predetermined data processing performance level independently of said performance control signal.